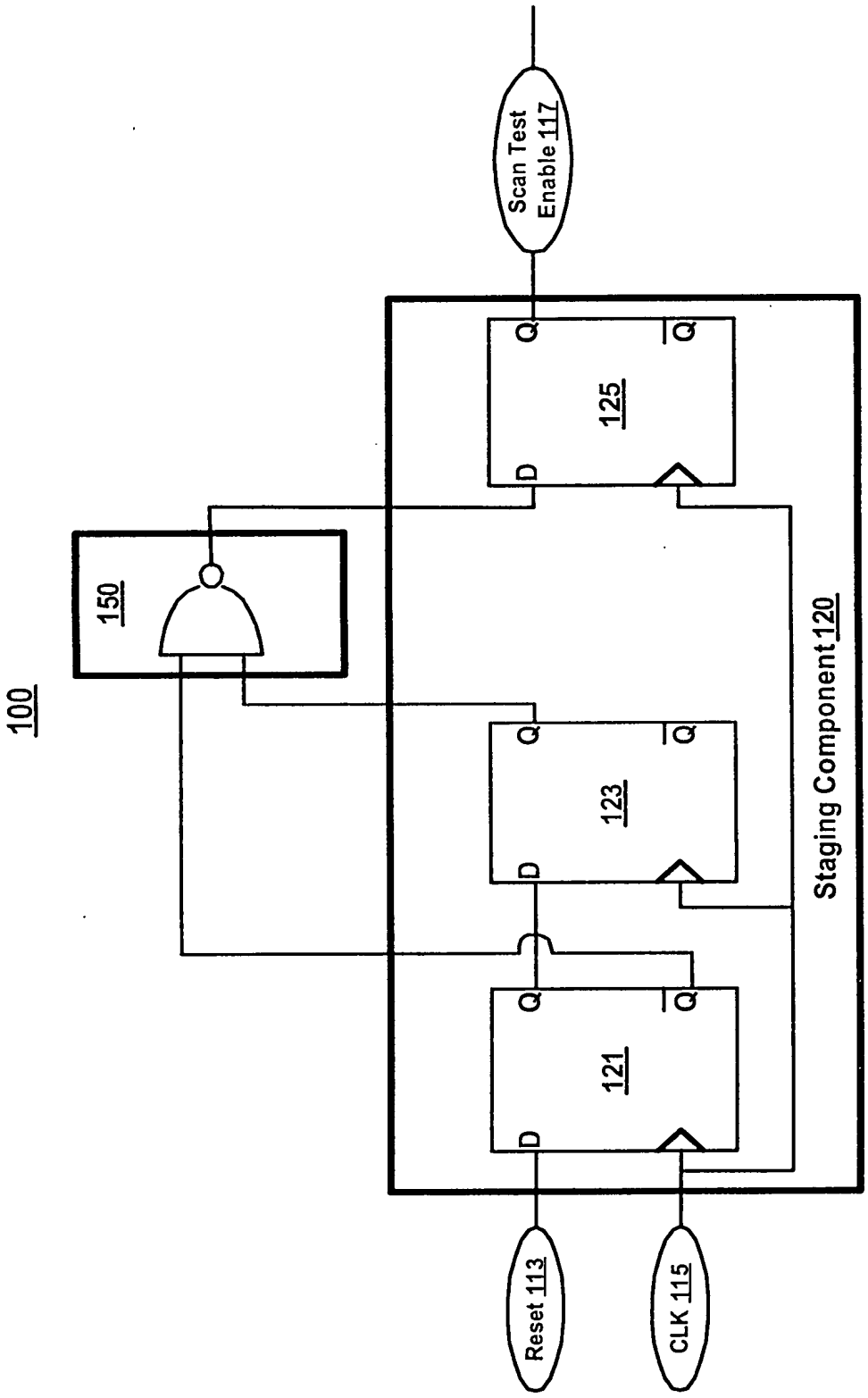

FIG. 1A

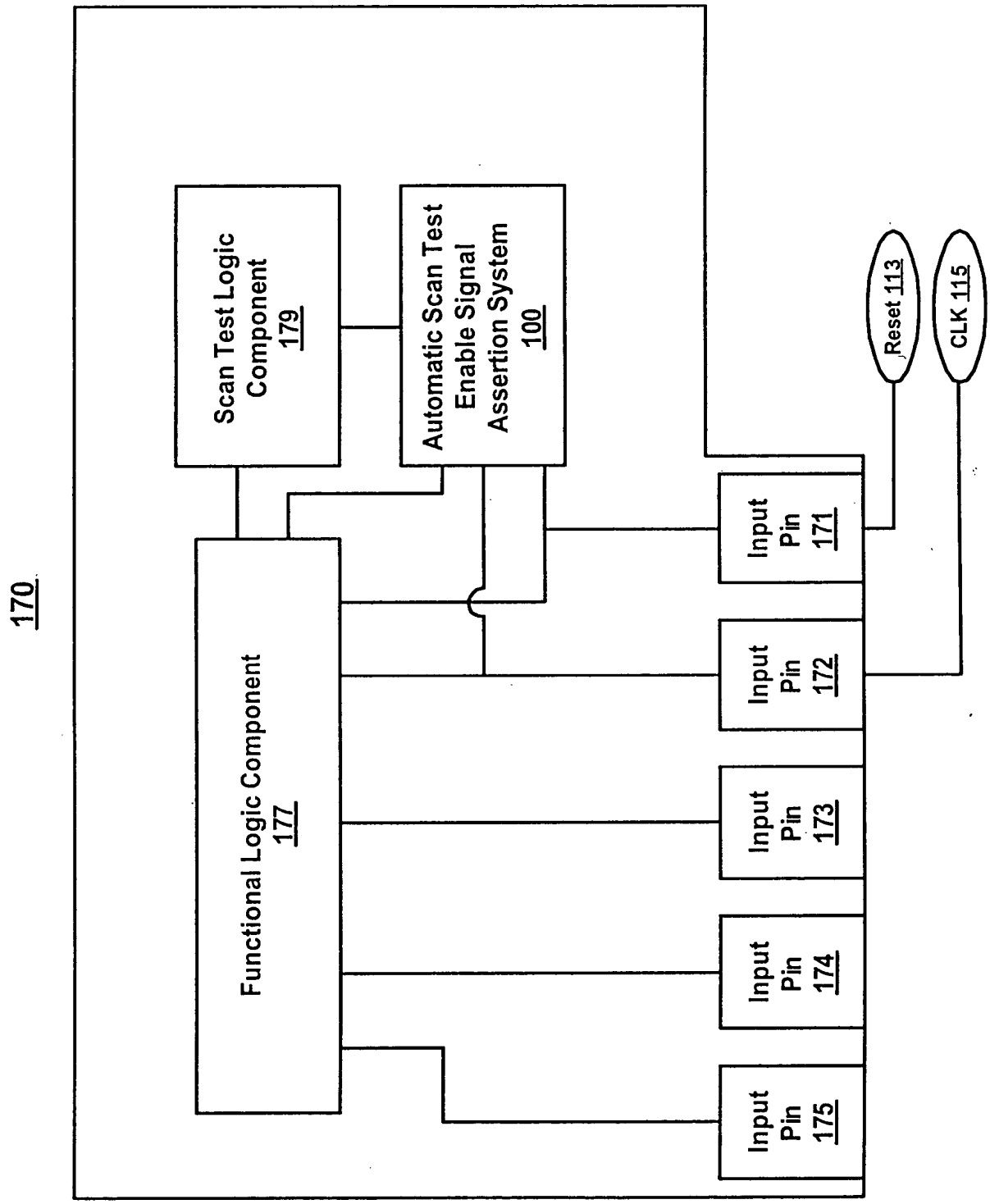

FIG. 1B

200

```
/ ****************************************
* *              BScanEnBlk Module              * *
**-------------------------------------         * *
**************************************** /
/  /-------------------------------------------------------------------------
module  BScanEnBlk (BScanEnbN,                    / / Output
                    pciClk, ioRstN );   / /Input
/  /-------------------------------------------------------------------------
output  BScanEnbN ;
input   pciClk,  ioRstN ;
reg     Q1_ioRstN, Q2_ioRstN, BScanEnbN ;
/  /-----------------------------------Circuit ----------------------------
/ / Generating the BScanEnbN ;
always  @ (posedge pciClk  )
          begin
            Q1   ioRstN  <- ioRstN;
          end
always  @ (posedge pciClk)
          begin
            Q2_ioRstN  <- Q1_iorstN ;
          end
wire      D_BScanEnbN        --(- Q1_ioRstN & Q2_ioRstN )   ;
always @ (posedge pciClk )
          begin
           BScanEnbN  <- D_BScanEnbN;
          end
endmodule
```

FIG. 2

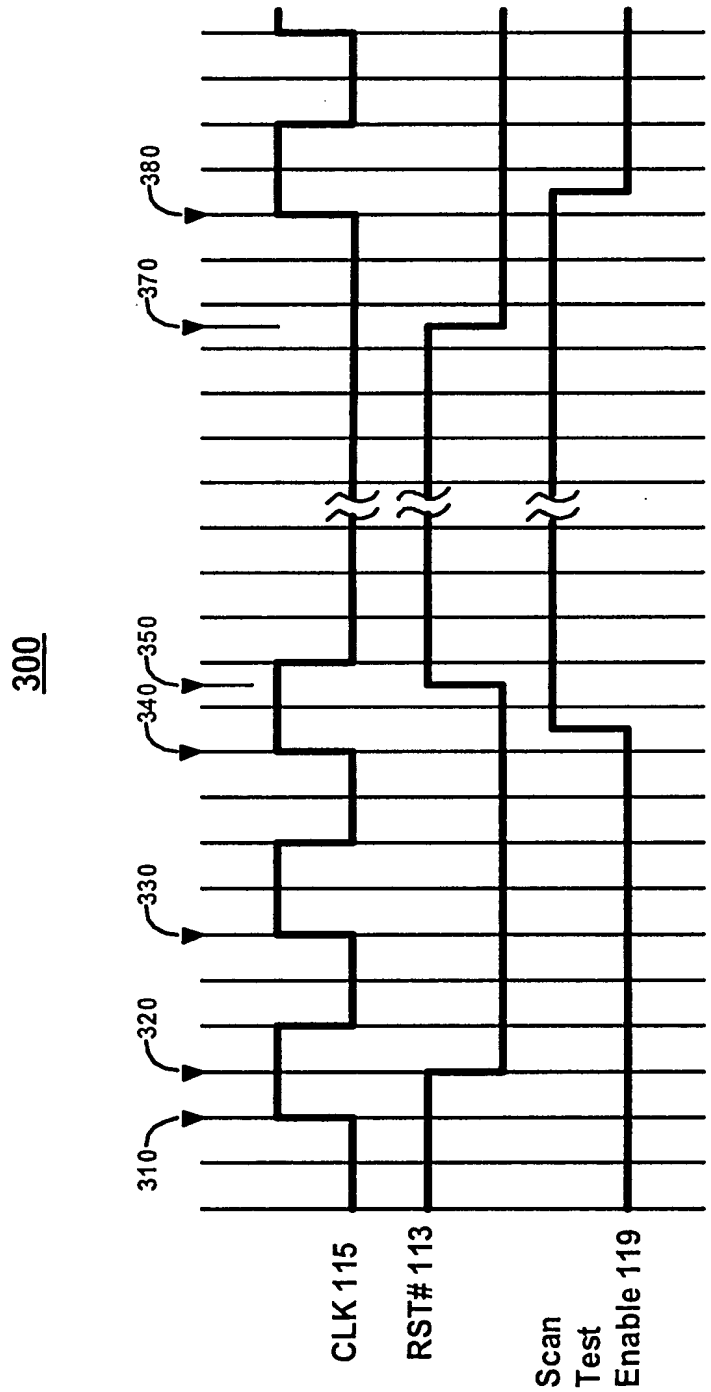

FIG. 3

400

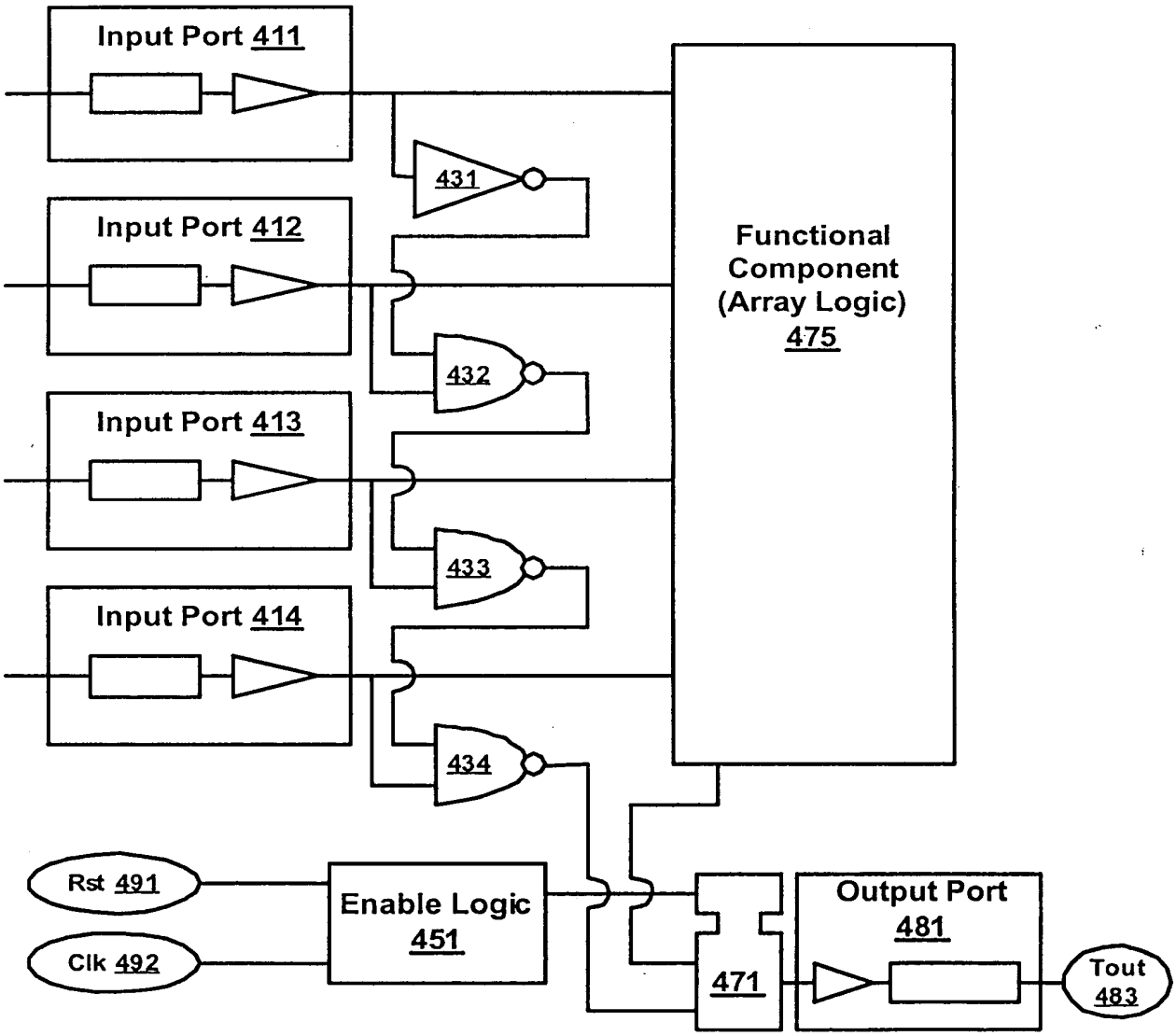

FIG. 4

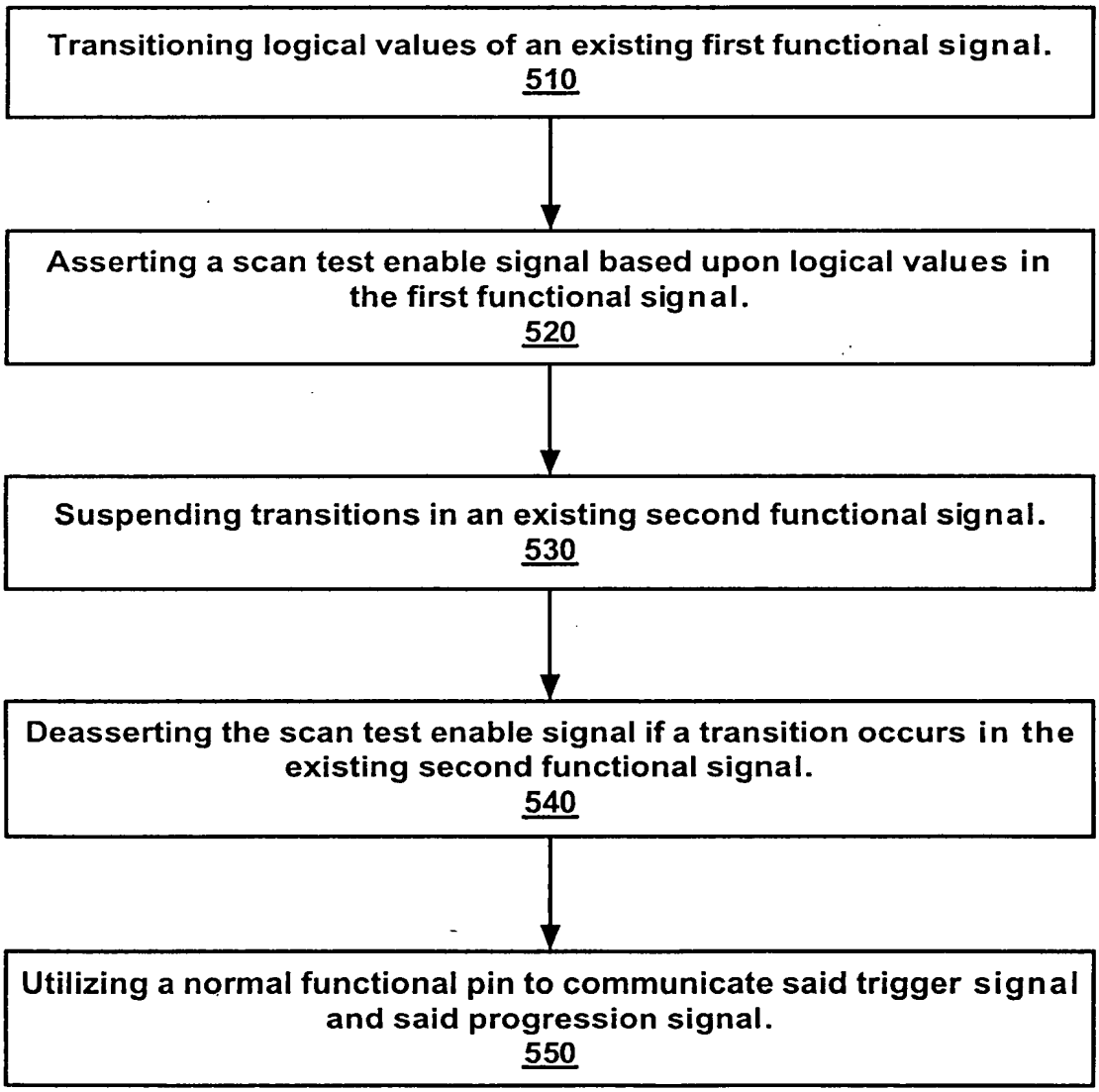

FIG. 5